Evaluation Board

FXPCTL is an evaluation board, designed for debugging and testing systems, which are built on the top of the FXP protocol. Evaluation board represents control cell that includes the protocol part as well as user resources.
Evaluation board includes the following:
Protocol part

- FX2 (CY7C68013-56PVC);
- DCU (XC2S50E-7TQ144C);
- PBM (XC9572XL-7TQ100C);
- A, B and C segment buffers (SN74ALVCH16245DL);
- EEPROM (24LC256-E/SM);
- FXP Bus (segment A) connector (IDC-64MS);

User part
Target FPGA XC2S50E-7TQ144C;

- Two seven-segment displays (SA56-21GWA);
- PLD-20 connector for general I/O (9 bit data, external CLK and 10 GNDD);
- Key connected to target FPGA.

Figure 1 describes functional diagram of FXPCTL evaluation board.

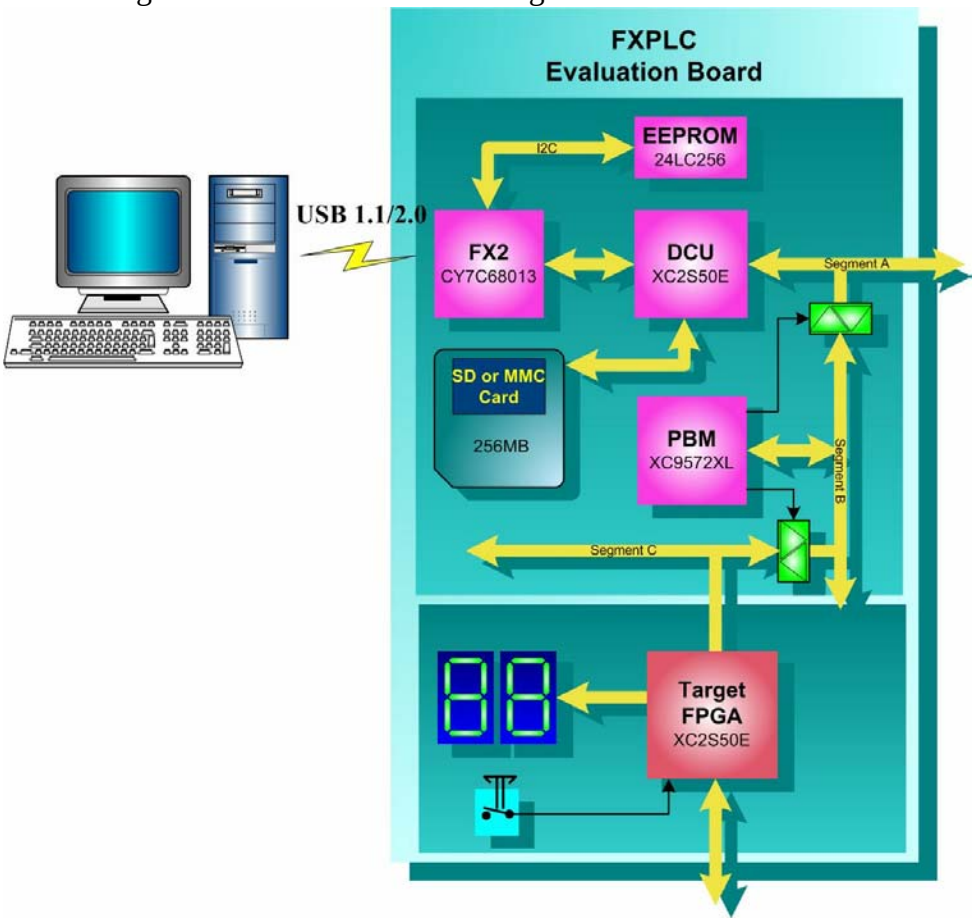

Figure 1

Top and bottom views are shown on the figure 2.

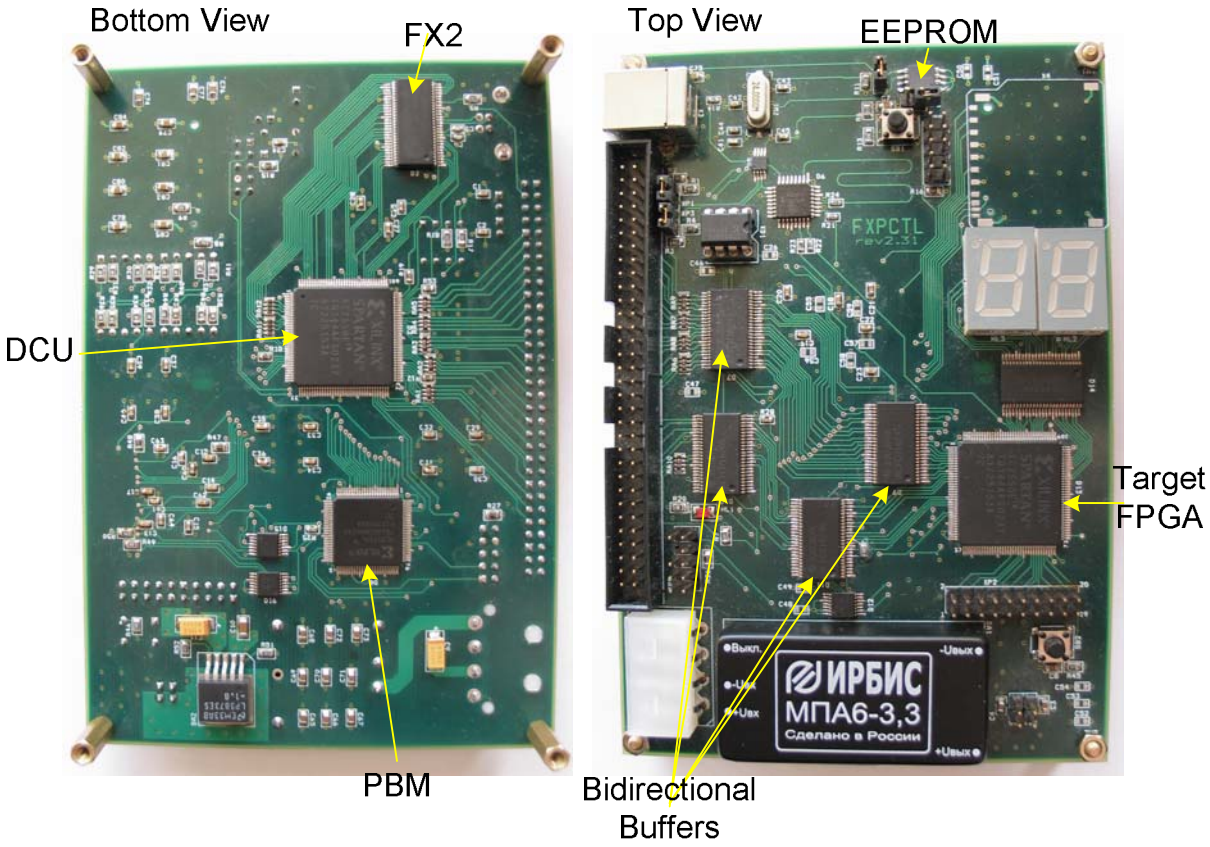

Figure 2

For the detailed information about FXPCTL Evaluation Board, refer to the Data Sheet section.